REMARKS

Claim Rejections – 35 USC §103

Claims 1-6, 9-16, 19-25, 28-35, & 38-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (US 20030084221, hereafter Jones), in view of ATA Packet Interface for CD-ROM (Revision 2.6 proposed, hereafter Pub).

Regarding claim 1, the applicant asserts that Jones in view of Pub does not teach all the features of claim 1 for at least the following reasons.

The applicant clarifies that the "predetermined interconnection means" as claimed in claim 1 is not the same as a port in claim 1. According to paragraph [0028] and Fig.6 of the disclosure, the controller 612 of the invention "is electrically connected to the single port 610 of the IDE/SATA channel 616" and "other peripheral devices can still be attached to a second port 618 of the IDE channel 616" (emphases added). From this, one can establish that the "predetermined interconnection means" of claim 1 is an IDE/SATA channel (in the current example), which is different from a port. Further to this point, an IDE/SATA channel (such as IDE/SATA channel 616) can have more than one port (610 and 618). As disclosed in paragraph [0005], the predetermined interconnection means "specifies the concept of channels and ports. Each channel in an IDE bus includes a first port and a second port and is normally associated with a single physical cable" (emphasis added).

Accordingly, the predetermined interconnection means (IDE channel) of claim 1 is "designed for providing the host access to a maximum of N devices", where N is 2 for an IDE channel. Applicant points to paragraph [0010] and Figs.4 and 5, stating "the IDE channel was designed to provide access to only two peripheral devices: a master and a slave" (paragraph [0010], emphasis added), one of which is connected to first port 410 and the other of which is connected to second port 412.

Claim 1 further claims "M peripheral devices electrically coupled to the controller; wherein M is greater than N and the controller allows the host to access the peripheral devices using the single port" (claim 1, emphases added). As an example, M can be 3, as depicted in

Fig.6: the three (M) devices 604, 606, 608 are electrically coupled to the controller 612, which is electrically coupled to the host 602 through a single port 610. In other words, the controller 612 is coupled to the host 602 using a single port 610 of a predetermined interconnection means (IDE channel) 616 which allows only a maximum of two devices, and the invention is shown to allow the host 602 to access three devices using that one port 610 which itself was designed for providing access to only a single device. Applicant points to paragraphs [0035] through [0037] describing allowing the host to access all devices through a single port, even when the original IDE/SATA channel was not designed to allow so many devices. By the same token, M can be 7, and the invention allows the host to connect to and access more devices than the general IDE interface was originally designed to allow.

Based on the above clarification, the applicant asserts Jones does not teach at least one of the claimed features of claim 1.

The Examiner has remarked that Jones discloses: "a controller electrically coupled to the host (chip 40 in Fig.9) through a single port 46 in Fig.9) of a predetermined interconnection means (IDE interface ¶[0046]), the predetermined interconnection means being designed for providing the host access to a maximum of N devices (IDE devices connected to the host by interface ¶[0046]); and M peripheral devices electrically coupled to the controller; (devices 62, 64, 66, 68, and 70 in Fig.9) wherein M is greater than N (host can choose which of the connected devices to access by chip 40 in Fig.9) and the controller allows the host to access the peripheral devices using the single port (chip 40 connects pc 20 through connector 46 all Fig.9)." (Office Action dated November 19, 2007).

To Jones, the predetermined interconnection means references the "IDE interface ¶ [0046]" (as pointed to by the Examiner), and Jones states there are a "total of 4 IDE ports" (paragraph [0039]) in a typical PC. In paragraph [0101], Jones further discloses "a Master slot and a Slave slot", referring to the two ports of a single IDE/SATA channel. As such, it is clear that Jones' use of the terms "connector", "slot", and "port" indicate the same element as the invention's disclosure of a "port" (as stated in claim 1). The present invention's disclosure of

"interconnection means" as defined in paragraph [0005] also indicates a concept similar to Jones's use of the term "IDE interface" as depicted in paragraph [0039]. Thus "port" and "interconnection means" are not the same thing, as an "interconnection means" comprises a plurality of ports (present paragraph [0005]) and Jones [0039] and [0101]).

Jones does not teach allowing the host to access M IDE peripheral devices through a single port, where M is more than the maximum number (being 4) of IDE devices that IDE was designed for providing access to. Applicant notes that the Master and Slave slots of Jones (each an IDE/SATA port) could originally only handle a single device: "IDE interface only supports one drive per connector" (paragraph [0101]). In paragraph [0111], Jones teaches "Master and Slave slots are expanded to handle multiple devices", and being able to connect two devices to a single connector (port) via IDE converter chip 40 with the commands taught in paragraphs [0102] through [0110]. According to paragraphs [0105] and [0110] of Jones, however, the only option for expanding is to identify "if the device is connected as Master slot" or "as a Slave slot". While Fig.9 of Jones shows multiple devices connected to the IDE converter chip 40, Jones only explicitly teaches allowing two devices– one identified as a Master, another as a Slave – through the single IDE connector, and the commands of paragraphs [0102] through [0110] explicitly limit the expandability. Jones does not enable a reader to allow the host to access more than two devices on this connector. A reader of normal skill in the art understands from Jones' commands that the two devices connected to IDE connector 46 occupy both the Master and Slave device allocations. Thus, the applicant contends that having Jones connected to one IDE connector for each IDE channel renders the other IDE connector of both channels unable to attach any devices. Since each IDE channel was already originally designed to handle a total of two devices, and there are two IDE channels in the IDE interface as defined by Jones, the total number of devices accessible is four. Therefore, implementing the teachings of Jones does not allow connecting more peripheral devices to the controller using a single port than the maximum number of devices the predetermined interconnection means was designed to provide access to, as claimed in claim 1.

Moreover, Jones also does not teach allowing the host to access all of "the peripheral devices using the single port" (claim 1). Due to the two-device limitation of Jones' commands, the host may only access two of the devices (only two of 62, 64, 66, and 68, for example) at any time. The remaining devices will be inaccessible to the host until the IDE controller disconnects one device in order to accommodate another. As above, Jones does not enable a person of normal skill in the field to allow the host to access all the connected peripheral devices exceeding two. By contrast, the present invention allows more than two devices to be concurrently accessible to the host by utilizing an implementation of virtual devices 812, such as those shown in Fig.10 and described in paragraph [0036], and applicant adds that the upper bound of such expansion is far beyond the originally designed IDE interface limitation.

Applicant summarizes, then, that Jones doe not teach M peripheral devices "coupled to the host through a single port of a predetermined interconnection means, the predetermined interconnection means being designed for providing the host access to a maximum of N devices" where "M is greater than N and the controller allows the host to access the peripheral devices using the single port".

As to "Jones does not disclose the host (Fig. 9 CPU 92) modifies predetermined existing fields in packets/commands" (Office Action dated November 19, 2007), it would not be obvious to a person of ordinary skill in the art to combine the teachings of Jones and Pub for at least the following reasons.

Due to the described limitations of Jones, combining the teachings of Jones with the proposed specification of Pub would not produce the novelties of the invention. What is more, there is neither suggestion nor motivation to combine the teachings of Jones with the proposed specification of Pub: doing so may allow modifying predetermined existing fields to identify the target device, but would still be subject to the two-device limitations of Jones, as described above.

Furthermore, as specified in Pub, the description mentioned by the Examiner states

that "operation codes so designated [as Reserved] ***shall not*** be used" and "are reserved for future extensions to this Specification" (Table 33, page 87). It would not be obvious and there would be no motivation for a person of ordinary skill in this field to use predefined fields wherein the specification expressly states the above.

From the above points and cited evidences, applicant affirms that neither Jones nor Pub nor an unmotivated combination of the two will teach all claimed features in claim 1. Therefore, applicant states that claim 1 should be found patentable over Jones in view of Pub. Likewise, independent claims 11, 20, 30, and 39 cover at least the same or similar claimed features, and as such should also be patentable for at least the same or similar reasons as were presented above for claim 1.

Furthermore, claims 2-8, 12-18, 21-27, 31-37, & 40-47 are dependent upon their base claims 1, 11, 20, 30, and 39, respectively, and should be found allowable for at least the same reasons as those presented for their corresponding base claims.

Claims 7, 8, 17, 18, 26, 27, 36, 37, & 45, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (US 20030084221), in view of ATA Packet Interface for CD-ROM (Revision 2.6 proposed), in further view of Fuller (US Pat# 4809164).

As mentioned, claims 7-8, 17-18, 26-27, 36-37, and 45-46 are dependent upon their base claims 1, 11, 20, 30, and 39, respectively, for which arguments have already been presented.

Furthermore, Fuller does not explicitly teach priority ranking that varies with any setting other than the speeds of the connected devices. On the other hand, the invention teaches that "the priority ranking can be a dynamic ranking that varies according to operations, such as write operations, or speed settings of the peripheral devices" (paragraph 0036 – emphases added). A device may have a plurality of speed settings which can affect its priority ranking and, by the same token, different operations such as read/write operations can also prompt a different priority for the device. The invention applies a dynamic priority

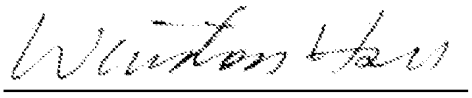
ranking according to the current needs of the device, which may be periodically or continually changing. In contrast, according to Fuller, the devices are assigned one of plural orders of priority, but the devices' priorities are not explicitly reordered based on the operations being processed. Fuller teaches that "higher priority is usually given to those devices that must unload data quickly to the high-speed devices, and the like, while a lower priority is given to slower devices" (column 2 lines 48-51 – emphases added). Applicant points that a priority ranking based on a "dynamic ranking that varies according to operations or speed settings of the peripheral devices" (claim 8) is different from lower priorities being given to slower devices, as taught by Fuller.

Consideration of claims 7-8, 17-18, 26-27, 36-37, and 45-46 is therefore respectfully requested.

Conclusion

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,



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